UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,986	05/25/2006	Bo Huang	42P22899	5991

45209 7590 07/13/2010

INTEL/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
MITCHELL, JASON D	

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
07/13/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,986	HUANG ET AL.	
	Examiner	Art Unit	
	Jason D. Mitchell	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/5/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an application filed on 5/25/06.

Claims 1-24 are pending in this application.

Claim Objections

Claim 1 is objected to because of the following informalities: line 5 recites "the plurality of first *figure* of merit". It is believed this should read "the plurality of first *figures* of merit". Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-12 and 21-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 1 fails to fall within a statutory category of invention. It is directed to a program itself (e.g. "A [software] system for evaluating … comprising: a first evaluator … and a binary selector"), not a process occurring as a result of executing the program, a machine programmed to operate in accordance with the program or a manufacture structurally and functionally interconnected with the program in a manner which enables the program to act as a computer component and realize its functionality. It's also clearly not directed to a composition of matter. Therefor it is rejected as being non-statutory under 35 USC 101.

Claims 2-12 depend from claim 1 and are rejected accordingly.

Claim 21 is not limited to statutory embodiments. In view of Applicant's disclosure, specification page 14, last full par., the claimed medium is not limited to statutory embodiments, instead being defined as including both statutory embodiments (e.g., Compact Disk Read-Only Memory (CD-ROMs), Read-Only Memory (ROMs), Random Access Memory (RAM), Erasable Programmable Read-Only Memory (EPROM)") and non-statutory embodiments (e.g., "a transmission over the Internet"). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

Claims 22-24 depend from claim 21 and are rejected accordingly.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4, 13-15, 19, 21 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by "Feedback-Directed Selection and Characterization of Compiler Optimizations" by Chow and Wu (Chow).

Claim 1: Chow discloses a system for evaluating and selecting programming code, comprising:

a first evaluator to measure a first characteristic of a plurality of input binaries (pg. 4, col. 2, 1st par. “Create a binary for each of the combination of the compiler switches”) and compute a plurality of first figures of merit for the plurality of input binaries, respectively (pg. 4, col. 2, 1st par. “Measure the performance for each binary"); and

a binary selector to compare the plurality of first figure of merit and select one of the plurality of input binaries as having the highest or lowest overall figure of merit (pg. 4, col. 2, 1st par. “Analyze results”; pg. 5, col. 1, 1st partial par. “Generate binary for the optimal set of switches”).

Claim 2: Chow discloses the system of claim 1 further comprising:

a second evaluator to measure a second characteristic of the plurality of input binaries and compute a plurality of second figures of merit for the plurality of input binaries, respectively (pg. 4, col. 2, 1st par. “Measure the performance for each binary"; pg. 2, col. 1, 1st par. “the program can be optimized for different purposes (e.g. speed, code size etc), the same method of experimental design can be applied."), wherein

the binary selector is to compare the plurality of second figures of merit (pg. 4, col. 2, 1st par. “Analyze results”).

Claim 4: Chow discloses the system of claim 2 further comprising:

a third evaluator to measure a third characteristic of the plurality of input binaries and compute a plurality of third figures of merit for the plurality of input binaries,

respectively, wherein the binary selector is to compare the plurality of third figures of merit (pg. 2, col. 1, 1st par. “Measure the performance for … (e.g. speed, code size etc)” those of ordinary skill in the art would have understood that this indicates the process is applicable to any number of 'figures of merit').

Claim 13: Chow discloses a machine-implemented method for processing computer programming code, comprising:

a) producing a current version of a binary using a current optimization setting (pg. 4, col. 2, 1st par. “Create a binary for each of the combination of the compiler switches”);

b) measuring a characteristic of the current version and computing a current figure of merit (FOM) associated with the current version (pg. 4, col. 2, 1st par. “Measure the performance for each binary");

c) comparing the current FOM with a previously computed FOM associated with a prior version of the binary (pg. 4, col. 2, 1st par. “Analyze results”); and

automatically repeating a)-c) for another optimization setting (pg. 4, col. 2, 1st par. “Create a binary for each of the combination of the compiler switches”).

Claim 14: Chow discloses the method of claim 13 further comprising:

indicating to a user the version of the binary that has the highest or lowest FOM as determined from the comparisons (pg. 5, 1st partial par. “Generate binary for the optimal set of switches").

Claim 15: Chow discloses the method of claim 14 further comprising:

ranking a plurality of versions of the binary in accordance with their respective FOMs as determined from the comparisons (pg. 5, 1st partial par. “the optimal set of switches").

Claim 19: Chow discloses the method of claim 13 further comprising:

d) measuring another characteristic of the current version and computing another figure of merit (FOM) associated with said another characteristic and the current version (pg. 2, col. 1, 1st par. “the program can be optimized for different purposes (e.g. speed, code size etc), the same method of experimental design can be applied.") ; and

e) comparing said another FOM with a previously computed FOM that is associated with said another characteristic and with a prior version of the binary (pg. 4, col. 2, 1st par. “Analyze results”).

Claim 21: Chow discloses an article of manufacture comprising:

a machine-accessible medium containing instructions that, when executed, cause a machine to:

a) generate a binary under an optimization setting (pg. 4, col. 2, 1st par. “Create a binary for each of the combination of the compiler switches”);

b) compute a cost as a function of a measured characteristic of the binary (pg. 4, col. 2, 1st par. “Measure the performance for each binary");

c) perform a) - b) a plurality of times each time with a different optimization setting but based on the same source program (pg. 4, col. 2, 1st par. "Create a binary for each of the combination of the compiler switches"); and

d) compare the computed costs, to select the binary having the lowest overall cost (pg. 4, col. 2, 1st par. "Analyze results"; pg. 5, col. 1, 1st partial par. "Generate binary for the optimal set of switches").

Claim 23: The article of manufacture of claim 21 further comprising instructions that cause the machine to perform b) by computing a further cost as a function of a measured, further characteristic of the binary generated in a) (pg. 2, col. 1, 1st par. "the program can be optimized for different purposes (e.g. speed, code size etc), the same method of experimental design can be applied.").

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 6-7 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Feedback-Directed Selection and Characterization of Compiler Optimizations" by Chow and Wu (Chow) in view of US 2004/0117779 to Lagergren (Lagergren).

Claim 3: Chow discloses the system of claim 2, but does not explicitly disclose the binary selector is to compute an overall figure of merit for each of the input binaries as a function of the input binary's first and second figures of merit.

Lagergren teaches computing an overall figure of merit for an input binary as the function of the input binary's first and second figures of merit (Lagergren par. [0025] "The output of the code introspection process is a number of factors, together with associated weights that are then used by the system in calculating the size metric").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to compute an overall figure of merit (Lagergren par. [0025] " factors, together with associated weights that are then used … in calculating the size metric") for each of Chow's .first and second figures of merit (e.g. pg. 2, col. 1, 1st par. "speed, code size"). Those of ordinary skill in the art would have been motivated to do so because optimization is system dependant and the overall figure of merit would allow for an application which was more finely tuned for the environment on which it is going to run (e.g. Lagergren par. [0025] "These factors reflect important parameters that the developer or system administrator should always know are an important factor in optimizing application code for this environment").

Claim 6: Chow discloses the system of claim 2 but does not disclose the binary selector is to compare the plurality of first and second figures of merit by computing a mathematical operation for each of the input binaries which includes the respective first and second figures of merit of that input binary.

Lagergren teaches comparing a plurality of first and second figures of merit by computing a mathematical operation for each of the input binaries which includes the respective first and second figures of merit of that input binary (Lagergren par. [0025] " factors, together with associated weights that are then used … in calculating the size metric").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to compute an overall figure of merit (Lagergren par. [0025] " factors, together with associated weights that are then used … in calculating the size metric") for each of Chow's .first and second figures of merit (e.g. pg. 2, col. 1, 1st par. "speed, code size"). Those of ordinary skill in the art would have been motivated to do so because optimization is system dependant and the overall figure of merit would allow for an application which was more finely tuned for the environment on which it is going to run (e.g. Lagergren par. [0025] "These factors reflect important parameters that the developer or system administrator should always know are an important factor in optimizing application code for this environment").

Claim 7: Chow and Lagergren teach the system of claim 6, wherein the first and second measured characteristics are selected from the group consisting of: performance (Chow pg. 2, col. 1, 1st par "speed"), code size (Chow pg. 2, col. 1, 1st par. "code size"), power consumption, compressed file size, and memory footprint.

Claim 24: Chow discloses the article of manufacture of claim 23 but does not disclose the instructions cause the machine to compare the computed costs in d), by computing an overall cost for each generated binary, wherein the overall cost is a function of said cost and said further cost computed in b).

Lagergren teaches comparing computed costs by computing an overall cost for a generated binary, wherein the overall cost is a function of a cost and a further cost (Lagergren par. [0025] " factors, together with associated weights that are then used … in calculating the size metric").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to compute an overall figure of merit (Lagergren par. [0025] " factors, together with associated weights that are then used … in calculating the size metric") for each of Chow's .first and second figures of merit (e.g. pg. 2, col. 1, 1st par. "speed, code size"). Those of ordinary skill in the art would have been motivated to do so because optimization is system dependant and the overall figure of merit would allow for an application which was more finely tuned for the environment on which it is going to run

(e.g. Lagergren par. [0025] “These factors reflect important parameters that the developer or system administrator should always know are an important factor in optimizing application code for this environment”).

Claims 5 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over “Feedback-Directed Selection and Characterization of Compiler Optimizations” by Chow and Wu (Chow) in view of US 5,901,310 to Rahman et al. (Rahman).

Claim 5: Chow discloses the system of claim 2 wherein the first characteristic is performance (pg. 2, col. 1, 1st par "speed”), and the second characteristic is file size (pg. 2, col. 1, 1st par. “code size”).

Chow does not explicitly disclose the second characteristic is compressed file size.

Rahman teaches that compressed file size is an important characteristic of a binary (col. 1, lines 48-51 “virtually increases the size of the nonvolatile semiconductor memory …. by storing the firmware in compressed form”).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to measure and optimize Chow's binary for compressed size (Chow pg. 2, 1st par. the program can be optimized for … code size etc”; Rahman col. 1, lines 48-51 “storing the firmware in compressed form”). Those of ordinary skill in the art would have

been motivated to do so to ensure a binary requires as less storage space (Chow pg. 2, 1st par. the program can be optimized for … code size etc"; Rahman col. 1, lines 48-53 "permits the firmware memory to hold more instructions than would otherwise be possible").

Chow and Rahman do not explicitly teach that the greater the performance or the smaller the compressed file size the smaller the associated figure of merit.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to associate a smaller figure of merit with a better performing binary (e.g. execution time) and a smaller figure of merit with a smaller compressed file size (e.g. compressed file size). Those of ordinary skill in the art would have been motivated to do so because the preferred figures of merit (Chow pg. 4, col. 2, 1st par. "Measure the performance for each binary") can have only a larger or smaller value (the disclosed ranking is a liner value indicating more optimal or less optimal), and either choice would allow a comparison to be made (Chow pg. 4, col. 2, 1st par. "Analyze results"). In other words ranking the figures of merit from large to small or small to large presents only a finite number of identified and predictable solutions within the ordinary level of skill in the art, and either solution would provide the necessary functionality.

Claim 20: Chow discloses the method of claim 13 but does not disclose the binary comprises a firmware driver, and the characteristic is compressed file size of the binary.

Rahman teaches that compressed file size is an important characteristic of a firmware driver (col. 1, lines 48-51 "virtually increases the size of the nonvolatile semiconductor memory …. by storing the firmware in compressed form").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize a firmware driver for compressed size (Chow pg. 2, 1st par. the program can be optimized for … code size etc"; Rahman col. 1, lines 48-51 "virtually increases the size of the nonvolatile semiconductor memory …. by storing the firmware in compressed form") using Chow's system. Those of ordinary skill in the art would have been motivated to do so to minimize the amount of storage space, and thus the cost, required for the driver (Rahman col. 1, lines 48-51 "virtually increases the size of the nonvolatile semiconductor memory …. by storing the firmware in compressed form"; col. 1, lines 25-27 "Providing a larger ROM bears a greater cost").

Claims 8-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Feedback-Directed Selection and Characterization of Compiler Optimizations" by Chow and Wu (Chow) in view of US 2004/0117779 to Lagergren (Lagergren) in view of Applicant Acknowledged Prior Art techniques (AAPA).

Claim 8: Chow and Lagergren teach the system of claim 7 further comprising:

a code generator that includes a compiler to process an output of the compiler and produce the input binaries (Chow col. 5, 1st full par. “the selected switch combinations can be fed to the compilation system to generate a binary"), wherein

the compiler exposes an optimization control to its user selected from the group consisting of: loop-unrolling (Chow pg. 2, col.1, 2nd par. "loop-unrolling transformation"); vectorization; and constant propagation.

Chow and Lagergren do not explicitly teach a code generator that includes a linker to process the output of the compiler.

The applicants acknowledge that it was known in the prior art to process the output of a compiler with a linker in order to generate a binary file (see e.g. pg. 1, last par. “A code generator may have the following components. A compiler … a linker joins the object files … into a binary image”).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a compiler and a linker in combination to generate Chow's binary files (Chow col. 5, 1st full par. “the compilation system to generate a binary"). Those of ordinary skill in the art would have been motivated to do so because this is the standard method of generating binary files (AAPA pg. 1, last par. “A code generate may have the following components. A compiler … a linker joins the object files … into a binary image”).

Claim 9: Chow and Lagergren teach the system of claim 8 but do not teach wherein the code generator further comprises a binary rewriter to process an output of the linker and produce the input binaries, wherein the binary rewriter exposes an optimization control to its user selected from the group consisting of: constant propagation; code shrinking; and specialization.

The applicants acknowledge that binary rewriters exposing an optimization control to its user selected from the group consisting of constant propagation; code shrinking; and specialization were known in the prior art (par. bridging pp. 9-10 "The binary rewriter 304 may be a conventional, binary rewriting tool ... Example optimization controls include constant propagation; code shrinking and specialization").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a prior art binary rewriter in Chow's system. Those of ordinary skill in the art would have been motivated to do so as another known method of applying optimizations to the code which would have resulted in only the expected results.

Claim 11: Chow and Lagergren teach the system of claim 7 but do not teach a binary rewriter to produce the input binaries based on a source binary, wherein the binary rewriter is to expose optimization controls to its user.

The applicants acknowledge that binary rewriters exposing an optimization control to its user were known in the prior art (par. bridging pp. 9-10 "The binary rewriter 304 may be a conventional, binary rewriting tool ... Example optimization controls include constant propagation; code shrinking and specialization").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a prior art binary rewriter in Chow's system. Those of ordinary skill in the art would have been motivated to do so as another known method of applying optimizations to the code which would have resulted in only the expected results.

Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Feedback-Directed Selection and Characterization of Compiler Optimizations" by Chow and Wu (Chow) in view of US 2004/0117779 to Lagergren (Lagergren) in view of Applicant Acknowledged Prior Art techniques (AAPA) in view of US 2006/0064676 to Chavan (Chavan).

Claim 10: Chow, Lagergren and AAPA teach the system of claim 8 further comprising:

configure the code generator in accordance with a plurality of optimization combinations, wherein the code generator is to produce the input binaries as configured by the optimization combinations, respectively (Chow pg. 5, col. 1, 1st full par. The selected switch combinations can be fed into the compilation system that generates binaries").

Chow, Lagergren and AAPA do not teach a script processor to process an input script from the user, the script processor to read a plurality of optimization combinations from the input script and configure the code generator in accordance with the optimization combinations.

Chavan teaches a script processor to process an input script containing a plurality of optimization combination to configure a code generator in accordance with the optimization combinations (par. [0043] “script 432 can ... invoke compiler 414 with ... compiler optimization options enabled … to generate optimized object code 422”).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a script (Chavan par. [0043] “script 432”) to feed Chow’s selected switch combinations to the compilation system (Chow pg. 5, col. 1, 1st full par.). Those of ordinary skill in the art would have been motivated to do so as a means of automating the disclosed functionality (i.e. Chow pg. 5, col. 1, 1st full par. The selected switch combinations can be fed into the compilation system that generates binaries").

Claim 12: Chow, Lagergren and AAPA teach the system of claim 11 further comprising;

a plurality of optimization combinations (Chow pg. 5, col. 1, 1st full par. The selected switch combinations can be fed into the compilation system that generates binaries") to configure the binary rewriter in accordance with the optimization

combinations, wherein the binary rewriter is to produce the input binaries as configured by the optimization combinations, respectively (AAPA par. bridging pp. 9-10 "The binary rewriter 304 may be a conventional, binary rewriting tool ... Example optimization controls include constant propagation; code shrinking and specialization").

Chow, Lagergren and AAPA do not teach a script processor to process an input script from the user

Chavan teaches a script processor to process an input script containing a plurality of optimization combination to configure a code generator in accordance with the optimization combinations (par. [0043] "script 432 can ... invoke compiler 414 with ... compiler optimization options enabled … to generate optimized object code 422").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a script (Chavan par. [0043] "script 432") to feed Chow's selected switch combinations to the compilation system (Chow pg. 5, col. 1, 1st full par.). Those of ordinary skill in the art would have been motivated to do so as a means of automating the disclosed functionality (i.e. Chow pg. 5, col. 1, 1st full par. The selected switch combinations can be fed into the compilation system that generates binaries").

Claims 16-18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Feedback-Directed Selection and Characterization of Compiler

Optimizations" by Chow and Wu (Chow) in view of Applicant Acknowledged Prior Art techniques (AAPA).

Claim 16: Chow and AAPA teach the method of claim 13 wherein the current and another optimization settings include optimization controls for compilation (pg. 4, col. 2, 1st par. "the compiler switches"), linking (AAPA pg. 1, last par. "A code generator may have the following components. A compiler … a linker joins the object files … into a binary image"), and binary rewriting (AAPA par. bridging pp. 9-10 "The binary rewriter 304"), and wherein said producing comprises:

compiling source code (Chow pg. 5, col. 1, 1st full par. "the compilation system that generates binaries") and linking object files to produce an initial version of the binary (AAPA pg. 1, last par. "a linker joins the object files … into a binary image"), and rewriting the initial version into the current version (AAPA par. bridging pp. 9-10 "The binary rewriter 304"), using the current optimization setting (Chow pg. 5, col. 1, 1st full par. "the best switches can be fed to the compilation system to generate a binary").

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Chow and AAPA for the reasons given in the rejection of claims 8 and 9.

Claim 17: Chow and AAPA teach the method of claim 13 wherein the current and another optimization settings include optimization controls for compilation (Chow col. 5,

1st full par. “the selected switch combinations can be fed to the compilation system to generate a binary") and linking (AAPA pg. 1, last par. “a linker joins the object files … into a binary image”) , and wherein said producing comprises:

compiling source code and linking object flies to produce the current version of the binary, using the current optimization setting (Chow col. 5, 1st full par. “the selected switch combinations can be fed to the compilation system to generate a binary"; AAPA pg. 1, last par. “a linker joins the object files … into a binary image”).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Chow and AAPA for the reasons given in the rejection of claim 8.

Claim 18: Chow and AAPA teach the method of claim 13 wherein the current and another optimization settings (Chow pg. 4, col. 2, 1st par. “Create a binary for each of the combination of the compiler switches”) include optimization controls for binary rewriting, and wherein said producing comprises: rewriting an initial version of the binary into the current version, using the current optimization setting (AAPA par. bridging pp. 9-10 "The binary rewriter 304”).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Chow and AAPA for the reasons given in the rejection of claim 9.

Claim 22: The article of manufacture of claim 21 wherein the instructions cause the machine to perform a) - b) a plurality of times, by first compiling the source program (Chow pg. 4, col. 2, 1st par. “Create a binary for each of the combination of the compiler switches”) and then rewriting the binary a plurality of times (AAPA par. bridging pp. 9-10 "The binary rewriter 304”) and then recompiling the source program (Chow pg. 4, col. 2, 1st par. “Create a binary for each of the combination of the compiler switches”) and then rewriting the recompiled binary a plurality of times (AAPA par. bridging pp. 9-10 "The binary rewriter 304”).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Chow and AAPA for the reasons given in the rejection of claim 9.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason D. Mitchell whose telephone number is (571)272-3728. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Bullock Lewis can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason D. Mitchell/
Primary Examiner, Art Unit 2193